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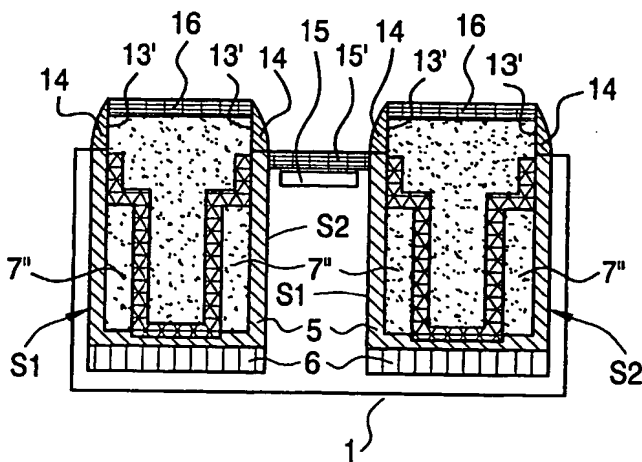
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(54) Title: NON-VOLATILE MEMORY CELL AND METHOD OF FABRICATION



(57) Abstract: Semiconductor device comprising
a vertical split gate non-volatile memory cell, for
storing at least one bit, on a semiconductor substrate,
comprising on the substrate a trench, a first active
area, a second active area, a channel region extending
along a sidewall of the trench, the trench having
a length extending in a first direction and a width
extending in a second direction perpendicular thereto
and the trench being covered on the sidewalls by a
tunnel oxide and including at least one gate stack of
a floating gate and a control gate, wherein the control
gate extends to the bottom part of the trench, a first
floating gate is located at a left trench wall to form a
first stack with the control gate, and a second floating
gate is located at a right trench wall to form a second
stack with the control gate.



— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X A	US 2002/096703 A1 (VORA MADHUKAR B) 25 July 2002 (2002-07-25) the whole document	1-4,15 5,14
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☒ Patent family members are listed in annex.

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